SAHIL SHAH

710 Peachtree Street NE, #501 ⋄ Atlanta, GA 30308
(+1 480 341 8399) ⋄ sshah389@gatech.edu ⋄ https://sahilshah21.weebly.com/

EDUCATION

Georgia Institute of Technology August 2014 - May 18
Candidate for Ph.D in Electrical Engineering
Thesis: Low-Power Computation Using FPAA for Wearable Devices

Arizona State University Fall 2011 - Spring 2014
M.S in Electrical and Computer Engineering
Thesis: Biosensors and CMOS Interface Circuits

Manipal Institute of Technology Aug 2007 - May 2011
B.E. in Electronics and Communication

RESEARCH AND WORK EXPERIENCE

Georgia Institute Of Technology Fall 14 - present
Graduate Research Assistant *Atlanta*

· I predominantly work on designing circuits and system on a mixed signal FPGA, which we call an FPAA, for processing the signals available from real world sensors (accelerometer, piezoelectric sensors, and MEMS microphone). This involves performing embedded machine learning by extracting features and classifying using single-layer of neural network. FPAAs have been designed by taking inspiration from neuromorphic computing and hence consume substantially low-power.

- Design and Layout of a mixed signal FPAA on 130nm technology node. (Both analog (ADC, DAC, Charge pump) and digital (MSP430 processor, GPIOs) components)
- Built-in Self-Test system for tuning GM-C filters and parameter on a large scale SOC.
- Temperature compensation and modeling on reconfigurable platform.
- Embedded classification on Field-Programmable Analog Array.

SophiaTech Summer 17 - Fall 17
Engineer *Atlanta*

· Stealth startup out of Georgia Tech (http://demoday.gatech.edu/2017/sophiatech/)

- Metal mask fix for Field Programmable Analog Array in 350nm technology.
- PCB design for handling power, UART communication via FTDI chip and clock.

Arizona State University Fall 11 - Spring 14
Graduate Research Assistant *Tempe*

· At ASU I worked on designing read-out circuits for CMOS based bio-sensors.

- Read out circuit for pH measurement consisting of ISFET (pH to I), transimpedance amplifier and 10 bit dual slope ADC (AMI 0.5 μm).
- Design and Layout of single ended switch capacitor circuit for glucose detection using fringed capacitance (AMI 0.5 μm).

RELEVANT PUBLICATIONS

· Sahil Shah ; Jennifer Hasler "**SoC FPAA Hardware Implementation of a VMM+ WTA Embedded Learning Classifier**" IEEE Journal on Emerging and Selected Topics in Circuits and Systems November 2017

- Sahil Shah; H. Toreyin; J.Hasler and A. Natarajan "**Temperature Sensitivity and Compensation On A Reconfigurable Platform**" IEEE Transactions on Very Large Scale Integration (VLSI) Systems briefs
- Jennifer Hasler; Sahil Shah, "**VMM + WTA Embedded Classifiers Learning Algorithm implementable on SoC FPAA devices**," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. PP, no. 99, pp. 1-1.
- Sahil Shah; Hakan Toreyin; Jennifer Hasler and Aishwarya Natarajan "**Models and Techniques for Temperature Robust Systems on a Reconfigurable Platform**" Journal of Low Power Electronics and Applications 2017, 7(3), 21.
- Sahil Shah; J. Hasler, "**Tuning of Multiple Parameters With a BIST System**," in IEEE Transactions on Circuits and Systems I: Regular Papers , vol. 64, no. 7, pp. 1772-1780, July 2017.
- S.Kim; Sahil Shah; J. Hasler "**Calibration of Floating-Gate SoC FPAA System**" IEEE Transactions on Very Large Scale Integration (VLSI) Systems vol. 25, no. 9, pp. 2649-2657, Sept. 2017.
- George, S.; Kim, S.; Sahil Shah et. al. "**A programmable and configurable mixed-mode FPAA SoC**", IEEE Transactions on Very Large Scale Integration (VLSI) Systems vol. 24, no. 6, pp. 2253-2261, June 2016.
- Sahil Shah; Smith, J.; Stowell, J. and Christen, J. B. (2015), '**Biosensing platform on a flexible substrate**', Sensors and Actuators B: Chemical 210, 197–203.
- Smith, J. T.; Sahil Shah; Goryll, M.; Stowell, J. R. and Allee, D. R. (2014), '**Flexible ISFET biosensor using IGZO metal oxide TFTs and an ITO sensing layer**', IEEE Sensors Journal 14(4), 937–938.
- Welch, D.; Sahil Shah; Ozev, S. and Christen, J. B. (2013), '**Experimental and simulated cycling of ISFET electric fields for drift reset**', IEEE Electron Device Letters 34(3), 456–458.

PATENTS

- Smith, J. T.; Goryll, M.; Sahil Shah; Blain Christen, J. and Stowell, J. (2015), "**System and Method for Ion-Selective, Field Effect Transistor on Flexible Substrate**", US Patent 20,150,330,941

AWARDS AND HIGHLIGHTS

- **Received best design award by Analog Devices Inc. at International Solid-State Circuits Conference (ISSCC) (2015)**
- Awarded Travel Scholarship to present research poster at Hardware and Algorithms for Learning On-a-Chip (HALO) workshop in Austin, Texas in 2015
- Marion A. and Henry C. Bourne Fellowship for attending Georgia Institute of Technology

WORKSHOPS

Mayo clinic: Demonstration of speech processing (Atlanta, August 2017)
Draper Labs: Demonstration of analog computation (Boston, December 2016)
Northrop Grumman: Demonstration on the use of FPAA (Washington DC, December 2014)

CMOS CHIP DESIGNS

- Cardiac processor for low-power acquisition of ECG signals and computing relevant features on **180nm** technology node. (Fall 2018)
- FPAA SoC metal mask FIX on **350nm** technology node at wafer level. (Fall 2017)
- Next generation FPAA SoC on **130nm** technology node with PLL, charge-pumps, ADCs, and DACs. (Fall 2016)
- Bio-sensing readout circuit with TIA and ADC on **500nm** technology node. (Spring 2014)
- Switch capacitor based glucose detection using fringed capacitance on **500nm** technology node. (Fall 2013)