A Real-Time Vital-Sign Monitoring in the Physical Domain on a Mixed-Signal Reconfigurable Platform

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***Abstract*—This work presents a mixed-signal physical-computation-electronics for monitoring three vital signs; namely heart rate, blood pressure, and blood oxygen saturation; from electrocardiography, arterial blood pressure, and photoplethysmography signals in** real-time**. The computational circuits are implemented on a reconfigurable and programmable signal-processing platform, namely field-programmable analog array (FPAA). The design leverages the core enabling technology of FPAA, namely floating-gate CMOS devices, and an on-chip low-power microcontroller to achieve energy-efficiency while not compromising accuracy. The custom physical-computation-electronics operating in CMOS subthreshold region, performs low-level (i.e., physiologically-relevant feature extraction) and high-level (i.e., detecting arrhythmia) signal processing in an energy-efficient manner. The on-chip microcontroller is used (1) in the programming mode for controlling the charge storage at the analog-memory elements to introduce patient-dependency into the system and (2) in the run mode to quantify the vital signs. The system has been validated against digital computation results from MATLAB using datasets collected from three healthy subjects and datasets from the MIT/BIH open source database. Based on all recordings in the MIT/BIH database, ECG R-peak detection sensitivity is 94.2%. The processor detects arrhythmia in three MIT/BIH recordings with an average sensitivity of 96.2%. The cardiac processor achieves an average percentage mean error bounded by 3.75%, 6.27%, and 7.3% for R-R duration, systolic blood pressure, and oxygen saturation level calculations; respectively. The power consumption of the ECG, blood-pressure and photo-plethysmography processing circuitry are 126 nW, 251 nW and 1.44 µW respectively in a 350nm process. Overall, the cardiac processor consumes 1.82 µW.**

***Index Terms*—energy-efficient cardiac signal processing, real-time physical signal processing, wearable sensor nodes**

I. Motivation for Real-Time and Energy-Efficient Cardiac Signal Processing

HEART disease (HD) is the primary reason for death in the U.S. and health care expenditure for HD imposes the largest burden on the total national health spending [1]. Furthermore, it is expected that by 2035, the percentage of the U.S. population having at least one HD will rise to 45%. Early diagnosis, and timely management of HD can potentially lower risk of complications, thus improving quality-of-life [1-4]. However, current HD diagnosis approach is reactive and therefore inappropriate for early diagnosis: Only after symptoms occur patients visit the clinic, where expensive procedures are used for diagnosis. In contrast, a proactive approach, where people are ubiquitously monitored at home for timely detection of signs of abnormalities before serious symptoms manifest, can increase the rate of early diagnosis. Such proactive approach can also facilitate treatment being tuned to changes in patients' physiology, thereby potentially increasing treatment success rates and reducing the frequency of visits to the clinic as well as the healthcare costs.

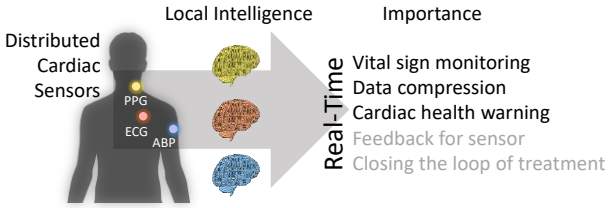

Fig. 1. This study presents design and results of energy-efficient physical computation electronics introducing real-time local intelligence to distributed cardiac sensors. Focus is given to ECG, ABP, and PPG signal processing. Energy-efficient and real-time vital sign monitoring, physiologically-relevant data compression, and cardiac health warning generation have been demonstrated on a mixed-signal reconfigurable FPAA platform.

Datasets collected from human-subject studies have shown that several critical hemodynamics and vital sign variables can be extracted from electrocardiography (ECG) [5], arterial blood pressure (ABP) [6], and photoplethysmography (PPG) [7] signals. Accordingly, several research groups and companies

Manuscript received July 8, 2019.

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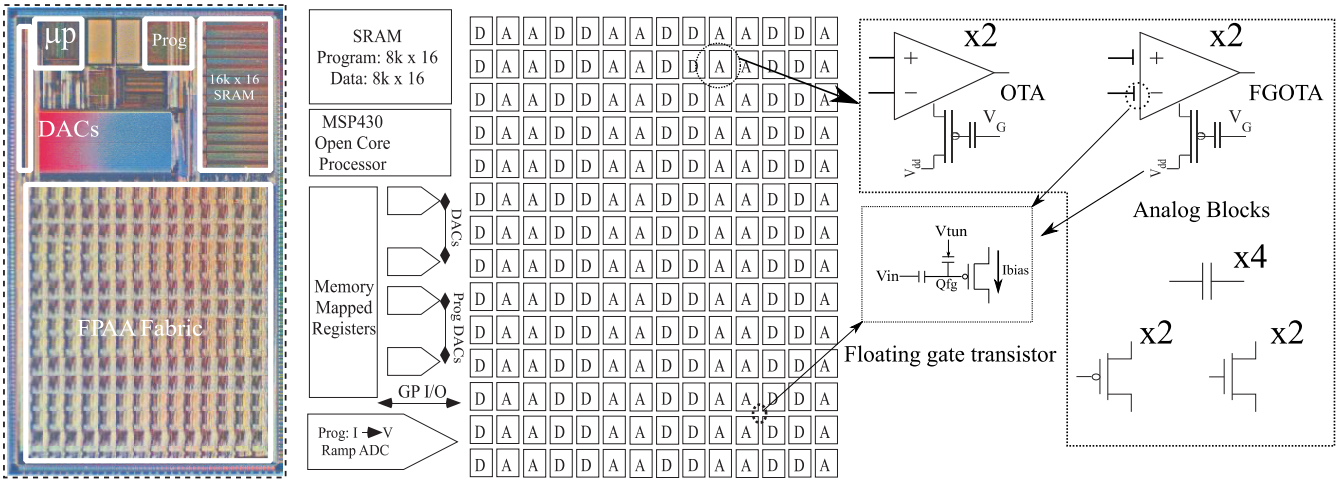

Fig. 2. Schematic and chip die of the Field Programmable Analog Array. The FPAA fabric consist of CABs and CLBs. These elements are programmed using the microprocessor and programming infrastructure. CAB element which are used in this work are also shown here. Interconnects, biasing of the OTA and inputs to the FGOTA are composed of Floating Gate (FG) transistors. The die photo of the FPAA SoC, fabricated in 350nm process, is also shown and has a dimension of 12 mm x 7 mm. An MSP430 micro-processor is also synthesized on the same die. The FPAA fabric and contents are from [8].

have developed wearable/implantable systems to capture and analyze those signals for cardiovascular health-assessment outside the clinic [9-15]. Majority of these devices consist of a (network of) sensor(s) collecting analog physiological data, which is digitized by a microprocessor (µP) for detailed offline analysis. But a µP consumes milliamperes of current and due to battery-life considerations, it is impractical to use µP for continuous processing of signals collected by sensor-nodes distributed across the body. Alternatively, a central processing unit with high computational power might receive and analyze the physiological data collected at different nodes. In such a scenario however, transmission of large datasets to the central processor necessitates high-throughput, and thus potentially power-hungry communication channels.

A potential solution to the aforementioned problem would be localized energy-efficient computation-nodes (Fig. 1). In a network with distributed and low-power computational capabilities, salient information could be extracted from the raw signals directly at the sensor site, thus significantly alleviating the burdens on the communication channel as well as the central signal processor. It should be noted that, in a body sensor network, physiological parameters of interest might change depending on the context. For instance, it is expected that the type and/or number of important physiological parameters during an exercise session (e.g., muscle activity) would be different than those during the activities of daily living. Therefore, a localized computation solution should offer adaptability to those changes to maximize the efficiency of resource-usage.

In this work, we present a proof-of-concept energy-efficient cardiac processor for analyzing cardiac signals in real-time. The focus of the paper is to demonstrate that custom analog-signal-processing algorithms implemented on a reconfigurable and programmable Field-Programmable Analog Array (FPAA) achieve superior energy-efficiency and resource usage performances compared to digital reconfigurable or programmable platforms. The energy efficiency is achieved because of (i) the design simplicity when implementing the signal processing functions using physical principles and (ii) facilitating the CMOS subthreshold region. The FPAA enables programmability and reconfigurability by leveraging Floating-Gate (FG) MOS devices.

This paper is organized as follows. In the following section, an overview of the FPAA platform, the cardiac signals of interest, and methods for evaluating the computation electronics are presented. Details of the electronics design and measurement results are presented in Section III, which is followed by a discussion in Section IV. The paper is concluded in Section V.

II. Methods: FPAAs for Analyzing Cardiac Signals

A. *FPAA: A Reconfigurable Mixed-Signal SoC*

There has been a growing interest in FPAA as a large-scale mixed-signal SoC. Similar to a Field Programmable Gate Array (FPGA) an FPAA makes prototyping mixed-signal systems cost effective and shortening the test cycles [16-17]. FG-based FPAAs [18-23] offer the required reconfigurability and programmability when implementing large analog systems typically suffering from mismatch and process variations [24,25].

The FPAA is shown in Fig. 2 and described in detail in [8]. It has both analog and digital blocks; namely Computational Analog Block (CAB) and Computational Logic Block (CLB); respectively. FPAA used in this work comprises of 98 CABs and 98 CLBs. These computational blocks are connected using Manhattan style routing composed of Connection (C) and Switch (S) blocks. These interconnect switches, which enable seamless connection between analog and digital blocks, are composed of nonvolatile FG transistors, show in Figure 2., which are programmed using hot-electron injection and globally erased using Fowler-Nordheim tunneling. The programming infrastructure used for tuning and programming the FG switches is composed of 7-bit DACs and a 14-bit ADC and are controlled using an open source MSP430 microprocessor. The microprocessor has a controllable

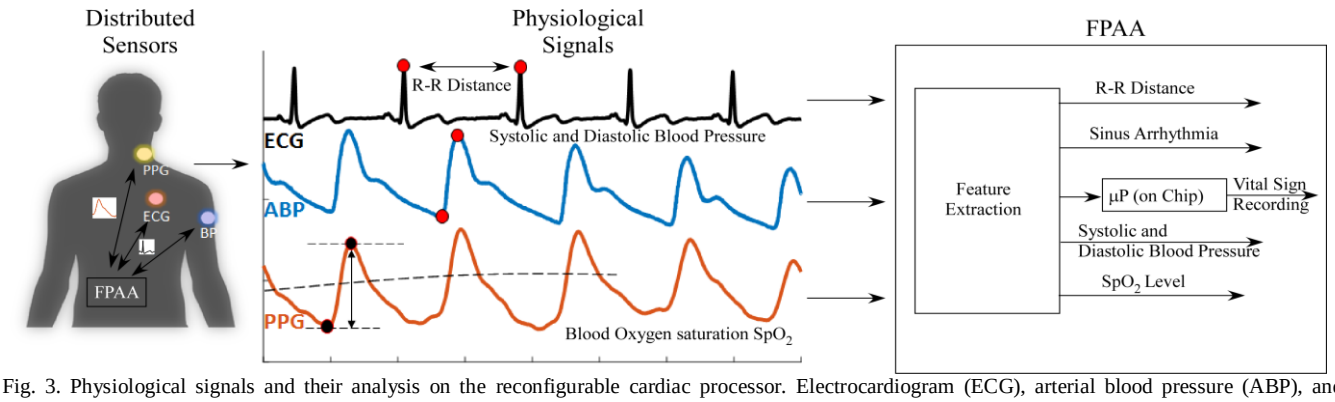

Fig. 3. Physiological signals and their analysis on the reconfigurable cardiac processor. Electrocardiogram (ECG), arterial blood pressure (ABP), and photoplethysmography (PPG) signal can be used for extracting important features and vital information are shown. Analog processing enables computation without using ADC, and hence significantly lower-power compared to the digital implementation of the algorithms. This is significant when such devices are used for continuous monitoring. The block diagram of the mixed-signal cardiac signal processor designed and implemented on an FPAA is also shown in the figure. The feature extraction and abnormality detection are performed in the physical domain, whereas vital sign value calculation is performed using the on-chip microprocessor.

frequency of 0-50 MHz and is synthesized on the same die as the FPAA fabric. An 8k x 16 bit SRAM is used to store the program to be executed by the microprocessor and a separate data memory of 8k x 16 bit is also present. As a part of the infrastructure there are sixteen 7-bit DACs for analog inputs to the FPAA fabric. The 14-bit ramp ADC, which is primarily used for measuring the current of a FG, can also be configured to digitize analog computation outputs.

Basic elements of a CAB, particularly the elements used in this work are shown in Figure 2. CAB elements are connected using local interconnects and the system use global routing while interconnecting to a different CAB. A CAB contains multiple Operational Transconductance Amplifiers (OTA) with the ability to select between wide linear range and high gain amplifier. Current bias of the OTA as well as the DC bias of the FGOTA is set using an FG transistor as shown in Figure 2. Similar to the interconnect switches, these FG transistors are programmed by a charge Q_{FG} using hot-electron injection and erased using Fowler-Nordheim tunneling. Unlike the interconnect switches, these FG transistors are programmed precisely to achieve the necessary biasing current (I_{bias}) [26]. The programming infrastructure enables programming the bias current values from 5 pA to 10 μA, and thus enabling calibration and tuning of the cardiac processor.

B. Overview of the Cardiac Signals and Features Critical for Vital Sign Calculation

The cardiac processor receives ECG, ABP, and PPG signals to compute R-R distance, systolic/diastolic blood pressure, and blood oxygen-saturation level (Fig. 3). In an ECG signal, R-wave, which is the global maxima point in a heartbeat, is critical for calculating the R-R distance, and therefore heart rate. In an arterial blood pressure (ABP) waveform, the maxima and minima points correspond to the systolic (SBP) and diastolic (DBP) blood pressure, respectively. Oxygen saturation (SpO2) can be calculated from two PPG signals at different wavelengths by calculating their perfusion index ratio. In this study, we use two commonly-used wavelengths, red and infrared (IR). The perfusion index of a PPG signal is calculated as the ratio of peak-to-peak PPG variations at different wavelengths respectively normalized by their corresponding dc levels.

C. Methods for Cardiac Signal Processor Validation

1) Physiological Datasets

The performance of the R-peak detection algorithm has been evaluated using all recordings in the MIT/BIH arrhythmia database [27-28]. In-case of, detection of R-R distance, SBP and DBP, and SpO_2 by the processor has been validated using datasets collected from three healthy adults. All measurements were approved by the Georgia Institute of Technology Institutional Review Board (IRB). The ECG dataset was collected using a wireless BioNomadix ECG module (Biopac Systems Inc., Goleta, CA). The ABP dataset was collected using a Finapres device (Finapres Medical Systems, Amsterdam, Netherlands) utilizing volume clamping technique for non-invasive and continuous blood pressure monitoring. The red and IR PPG dataset was collected using an AFE4400SPO2EVM pulse-oximeter evaluation-module (Texas Instruments, Dallas, TX). All signals were collected using a sampling rate of 2 kSps per channel. We followed a measurement protocol consisting of rest, handgrip exercise, and deep breathing phases and creating perturbations in heart rate (HR) and BP. During measurements, the subjects were in standing position.

For validation of the sinus arrhythmia warning generation circuitry, 10 minutes ECG recordings from three different adults (recordings 114, 210, and 214) in the MIT/BIH database have been used [27-28].

2) R-Wave Detection Algorithm Validation

The robustness of the R-wave detection algorithm has been validated using the simulation environment of the FPAA [29]. The environment facilitates an open source clone of MATLAB/SIMULINK, namely SCILAB/XCOS, and provides a graphical interface enabling simulations, rapid prototyping, and calibration. For all 48 ECG recordings of the MIT/BIH arrhythmia database, the first channels are used in this study. Each recording is fed to the simulation environment following digital signal conditioning to fit the signal into input rails of the processor. The simulation outputs are compared against the

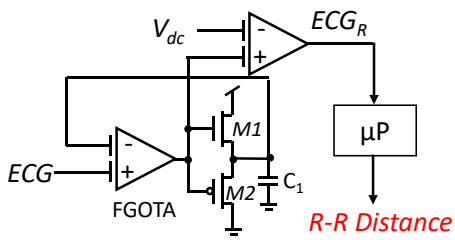

Fig. 4. ECG R-wave features are detected by a hysteretic differentiator followed by a voltage comparator. The output of the voltage comparator, which is a train of pulses, is fed to the microprocessor for finding the R-R distance. Consistency is observed in the exemplary waveforms displaying the R-R distance calculated by the on-chip microprocessor using the features detected by the circuit implemented on the FPAA fabric and MATLAB using the features found by MATLAB.

annotations in the database to extract the sensitivity (*Se*) using *Se=TP/(TP+FN)*, where *TP* and *FN* are respectively true positive and false negative values.

3) Cardiac Signal Processor Validation Setup on FPAA

For validation purposes, the waveforms have been streamed on to the FPAA using a 14-bit DAC. In an ultimate BSN cardiac sensing node scenario, sensors could be directly interfaced with the FPAA using either a low-noise amplifier or capacitively coupled amplifiers, depending on the type of the sensor/transducer.

For cardiac feature extraction accuracy assessment, the cardiac processor outputs have been compared with the outputs of digital signal processing algorithms implemented on MATLAB. Sinus arrhythmia detection performance of the processor has been evaluated through comparison with the arrhythmia events annotated on each ECG recordings.

III. Reconfigurable Cardiac Processor

A. Feature Extraction from Physiological Data for Vital Signs

1) ECG R-Wave Detection

The R-wave of a heartbeat, which is critical for heart rate calculation, is preceded and followed by points where the magnitude of the first derivative of the ECG signal is maximum. Therefore, the R-wave detection circuitry is designed to detect the sharp and large changes in the slope while suppressing the small changes such as noise. Accordingly, the R-wave detector algorithm is designed as a hysteretic differentiator with a time-constant set by the transconductance of an operational transconductance amplifier (OTA) and a load capacitance, C_1 (Fig. 4). FGOTA has an increased linearity as compared to a traditional non-FGOTA at the expense of gain [30]. The increased linearity of the FGOTA follows from the differential current given by the following equation:

$$Iout = I_{bias}\tanh(\kappa\frac{C_{in}}{C_T}\frac{V_{in1}-V_{in2}+V_{offset}}{2U_T}) \quad (1)$$

where V_{in1} and V_{in2} are differential input voltage of the FGOTA and V_{offset} is mismatch due to threshold voltage mismatch and FG charge programmed, C_{in} is input capacitor to the FGOTA and C_T is total capacitance at the FG node, κ is the fractional change in surface potential with respect to change in gate voltage, and U_T is thermal voltage which is approximately equal to 25 mV at room temperature. The additional term C_{in}/C_T, the ratio of input capacitance to the total capacitance at the input of

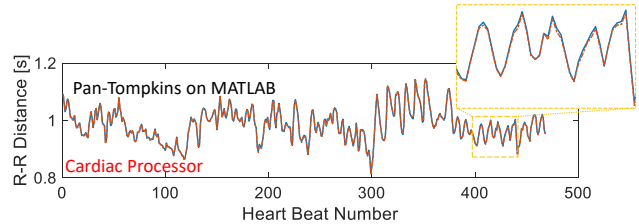

Fig. 5. The R-R distance calculated by the cardiac processor and Pan-Tompkins implementation on MATLAB match. The exemplary data corresponds to ECG data from a healthy subject.

the differential FGOTA, results in increased linearity over traditional non-FG OTA. Linearity of the FGOTA can be increased by increasing the total capacitance C_T [31]. The FGOTA is used as part of the hysteretic differentiator as seen in Fig. 4. Hysteretic differentiator's output is responsive only to major changes in sign of the derivative of the input voltage. Additionally, by changing the g_m (I_{bias}) of the FGOTA, noise immunity can be further enhanced by making V_{C1}, the voltage of C_1 in Fig. 4, to lag even further behind the input [32]. For small signals, the output of the hysteric differentiator in Figure 4 is governed by:

$$C_{out} * \frac{dVout}{dt} = G_m \times (V_{ECG} - V_{C1}) \quad (3)$$

where G_m is the transconductance of the FGOTA given by ($I_{bias}*\kappa*(C_{in}/C_T)/(2*U_T)$. The time constant in (3), given by $\tau=C_{out}/G_m$, is selected such that high-frequency noise above 50 Hz is suppressed specifically the 60-Hz noise. Using the parameters extracted in [33] $\kappa*(C_{in}/C_T)$=0.48 and C_{out}=1pF we get I_{bias} of 33pA. This value was then used as the basis for the Built-In-Self-Test (BIST) which tuned the biasing current to 0.1nA to obtain the specified 50 Hz bandwidth. The BIST architecture is similar to the one described in [34] and it takes into account the mismatch that arises from indirect programming of FG [26], differences in the load-capacitance and other mismatches that arise in CMOS process. The capacitor (C1) shown in Fig. 4 is local routing capacitance and has a value of 160fF. An FGOTA comparator converts the differentiator output into clock pulses fed to the microcontroller for calculation of the HR value. The FGOTA also allows us to precisely program the offset of the OTA and hence the comparator threshold could be configured depending on the subject. R-R distance calculated using the comparator outputs, ECGR, from ECG recordings of one of the healthy subjects, match with those calculated using the R-waves detected by the MATLAB implementation of the Pan-Tompkins algorithm [35] (Fig. 5). The on-chip µP counts the time between the rising edges of the ECG_R pulses, whereas the R-R distances of the Pan-Tompkins output are calculated using the R-wave peak points. Accordingly, small (< 1 ms) differences occur between the two data (close-up view in Fig. 5). The two results exhibit a Pearson correlation coefficient of 0.99.

2) ABP Feature Extraction

The SBP and DBP values; which are the maximum and minimum values of the continuous ABP waveform, respectively; are detected by an envelope tracking circuitry. The operation of the positive peak detection circuitry (Fig. 6) is as follows. When the input signal is greater than the output (i.e., ABP signal is increasing), the NMOS controlled by the FGOTA output charges the load capacitor, C_{L1}, thereby causing the output to follow the input. When the input is less than the

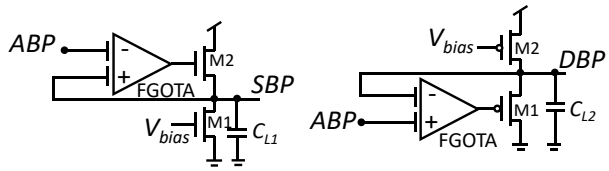

Fig. 6. SBP and DBP are detected from the ABP waveform via maximum and minimum detection circuitry, respectively.

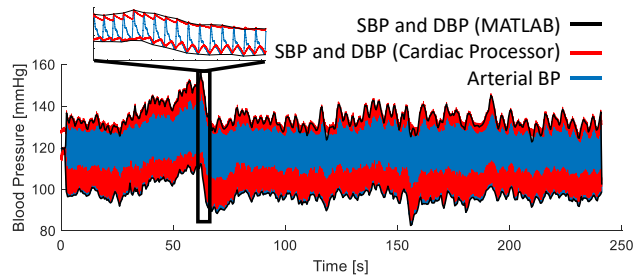

Fig. 7. Exemplary SBP and DBP waveforms obtained from the ABP of a healthy subject are shown. The SBP and DBP values obtained by MATLAB are also provided for comparison.

output, the NMOS controlled by a fixed bias voltage discharges the C_{L1} at a discharge rate given by I_1/C_{L1}, where I_1 is dependent on current through M1 and M2. We empirically selected the V_{bias} value for a maximum detector to limit the discharge rate such that the maximum value is held almost constant between successive heart beats, which can take as long as 1 sec (60 bpm). Likewise, we empirically selected bias currents for the FGOTAs such that the capacitor charge rate is sufficiently large to charge C_{L1} and track the input signal in less than 50 ms when the next heart beat arrives. The minimum peak detection circuitry differs from the positive peak detection circuitry by using PMOS instead of NMOS devices for generating the C_{L2} current. SBP and DBP signals obtained by the processor and MATLAB from an ABP waveform are presented in Fig. 7. The capacitors (C_{L1} and C_{L2}) and devices (M_1 in SBP circuitry and M_2 in DBP circuitry) affect the discharge rate. The bias voltage, V_{bias}, can be tuned to compensate for potential process variations in these elements. Similarly, by tuning the FGOTA bias current, potential process variations can be compensated to ensure the output can be ensured to follow the input before the maximum (SBP) and minimum (DBP) peaks.

3) PPG Feature Extraction

For monitoring the SpO_2, the cardiac processor calculates the ratio (R) of the perfusion indices (i.e., ratio of the pulsatile blood flow signal to static blood flow) of PPG waveforms at red and infrared wavelengths [36].

The perfusion-index-ratio extraction block consists of circuitry detecting the 1st order features, namely the peak-to-peak and dc values of red and infrared wavelength PPG signals; followed by an arithmetic operation circuitry for calculating the ratio of the perfusion indices (i.e., $R = \frac{V_{pp,red}}{V_{dc,red}} / \frac{V_{pp,ir}}{V_{dc,ir}}$) of red and infrared wavelength PPG signals. Peak-to-peak detection is achieved using the envelope detection circuitry described in the ABP feature extraction section. We follow the approach described in Section III.A.2 for the bias selection of the PPG envelope detection circuitry. The dc values of the PPG signals are detected through a low-pass-filter (LPF) implemented as a G_m-C stage with a time constant set to f_{-3dB}= 300 mHz by the transconductance of an FGOTA and a load capacitance (Fig. 8(a)). The time constants are tuned using a BIST method [34]. The BIST is used to automatically tune parameters to the desired values (e.g., the time constant for the LPF). The two-step calibration procedure used for an FPAA is detailed in Section 4. The time-constant is calculated using models simulated in MATLAB to achieve desired performance. The inputs to the next stage are output currents of wide input-linear-range (~ 1.5 V) FGOTAs fed by the voltage outputs of the envelope detection and LPF circuitry.

For ease of computation and therefore reduced design complexity, calculation of perfusion indices as well as their ratio is achieved in the analog domain using current signals. This is important from the standpoint of real-time monitoring system where the continuous use of analog to digital converter (ADC) will increase the power consumption. The overall calculation is reduced into a single translinear multiplier/divider circuitry using multiple input translinear elements (Fig. 8(b)), where the output current, Iout, is dependent to I1-to-I4 through:

$$I_{out} \propto (I_1 I_2)/(I_3 I_4). \quad (2)$$

The relationship in (2) follows from the drain current for FG pMOS in subthreshold regime operated in saturation, and the

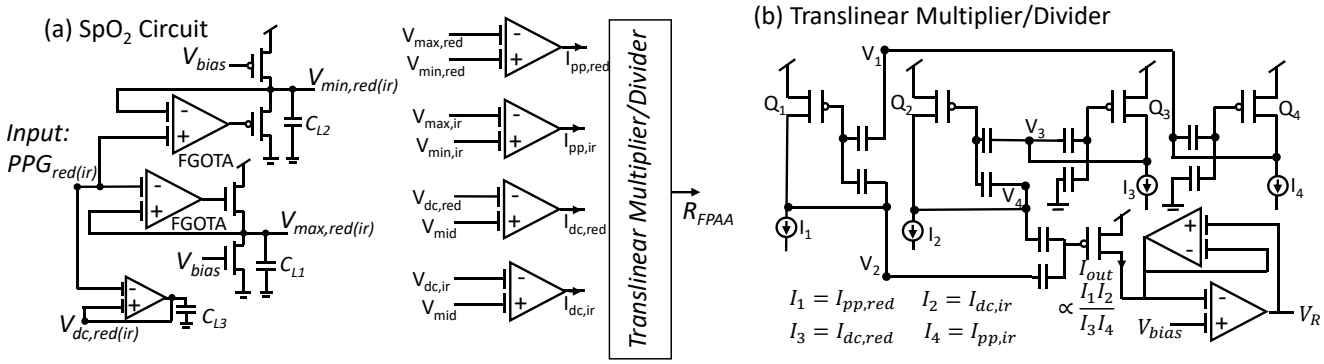

Fig. 8. (a) SpO_2 calculation circuitry. To calculate the peak-to-peak and dc value parameters required to calculate the perfusion indices of red and infrared wavelength PPG signals, max-min detect and G_mC LPF stages are designed, respectively. The voltage outputs are converted into current at FGOTAs to achieve the (b) perfusion index ratio operation in the current domain using a translinear current multiplier/divider implemented using multiple-input translinear elements (MITEs).

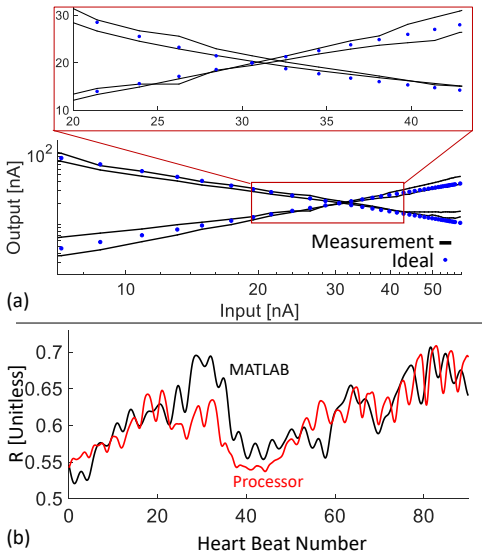

Fig. 9. (a) Measurement results for the translinear circuit output (I_{out}) vs. input (I_1) current for two I_2 and two I_4 values are presented. During operation, I_1-I_4 are limited to 20 nA – 43 nA, where the circuit is linear. (b) The perfusion-index-ratio waveforms obtained by the cardiac processor and MATLAB. The smoothed waveforms follow similar trends and have similar peaks and valleys.

fact that current is mirrored [37,38]. The following equations illustrates the relationship between input current and output currents:

$$I_{out} = I_{th} * e^{\frac{\kappa(V_{DD}-w_{V2}-w_{V4}-V_{th})}{U_T}} \quad (3)$$

$$I_{out} \propto e^{\frac{-w_1 V_2}{U_T}} * e^{\frac{-w_1 V_4}{U_T}} \quad (4)$$

where w1 is the product of κ and FG weight w. V2 and V4 are as shown in Fig. 8(b) and can be replaced in terms of current I1, I2, I3 and I4. The relation for an FG drain current with respect to FG voltages for Q1 is given as follows:

$$V_2 \propto -\ln(I_1)\frac{U_T}{w1} - V_1 \quad (5)$$

Similar relation can be written for Q2, Q3 and Q4 transistors in Fig. 8. Replacing equation (5) in (4) we get

$$I_{out} \propto e^{\frac{-w1}{U_T}(-ln(I_1)\frac{U_T}{w1}+ln(I_4)\frac{U_T}{w1})} * e^{\frac{-w1}{U_T}(-ln(I_2)\frac{U_T}{w1}+ln(I_3)\frac{U_T}{w1})} \quad (6)$$

Reducing the above equation, we get the relation in (2). The above relation and the linearity hold true only if the charges programmed on the FGs are equal and the FGs are matched. The I_{out} is converted into voltage, V_{out}, at a transimpedance stage implemented as an OTA with an FGOTA-buffer feedback resistance (Fig. 8(b)). Linearity of the translinear elements and comparison of processor output, V_R, and digital MATLAB calculations of the perfusion-index-ratio are presented in Fig. 9.

B. *Sinus Arrhythmia Detection from ECG*

Sinus arrhythmia manifests itself as irregular R-R intervals, resulting in prolonged R-R intervals for some heart beats [39]. In this proof-of-concept algorithm, we aim to detect abnormal increases in R-R intervals. To detect such irregularity, the R-R interval is first time-integrated using a peak-detector circuitry (Fig. 10). To a first order approximation, charge leakage of the load capacitor can be modelled as a constant current source

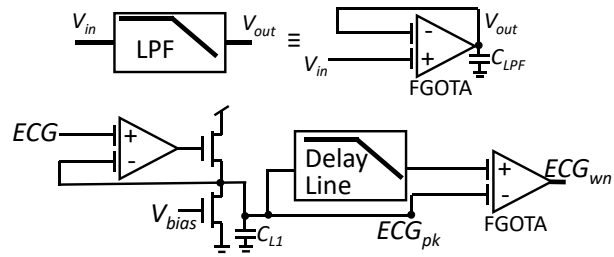

Fig. 10. Sinus arrhythmia detection circuitry. The maxima waveform of an ECG signal, which is tracked by a peak detection circuitry, is fed to a comparator. The threshold for the comparator is a delayed version of the ECG maxima waveform.

reducing the C_{L1} potential by an amount proportional to the R-R interval between successive peaks. The output of the peak-detector is compared with an adaptive threshold at a comparator to generate a warning pulse in the event of abnormally long R-R interval. The adaptive threshold value is selected such that false positives during normal gradual R-R interval increases (e.g., drops in the HR following deep breathing or exercise) are prevented while abrupt increases (occurring within < 1 s) in the R-R interval are detected as arrhythmia events. The adaptive threshold is created as the one second delayed and smoothed version of ECG_{pk} signal. The delay network consists of eight cascaded LPF G_mC stages (Fig. 10).

Notably, arrhythmia events can be detected using the ECG-R wave circuit (Figure 4) in conjunction with the microprocessor. In that case, it would require several registers to store previous set of values and digital logic to detect sudden changes in R-R distance. On the contrary, the proposed circuit in Figure 10 enables detection of arrhythmia without having to use a digital counter, the registers for storing previous set of R-R distance, or logic circuitry to detect the sudden change in those values.

C. *Vital Sign Data Logging*

The on-chip low-power MSP430 microprocessor with an energy efficiency of 216 µW/MHz is used to calculate and log some of the physiological signals. For demonstration purposes, we use GPIO (General Purpose Input- Output) to continuously poll for an event to occur. In general, the processor could be used in an interrupt mode, where an event generated by the FPAA fabric would be used to wake-up the processor.

R-R interval for ECG is calculated using a simple counter implemented on the processor in conjunction with the FPAA fabric. Assembly code is used to reduce the size of the SRAM cell needed to store the algorithm and in turn reduce the power consumption.

IV. Cardiac Processor Validation and Discussion

The FPAA R-wave detection algorithm simulations, which were performed using the models generated for the devices on the FPAA [33], resulted in an average sensitivity of *Se*=94.2% for the 48 recordings in the MIT-BIH arrhythmia database. The cardiac processor outputs that timestamp abnormally long R-R sinus arrhythmia events are presented in Fig. 11. Red dots in Fig. 11 represent all beats with arrhythmia events such as premature ventricular contractions and rhythm changes in addition to degraded signal quality, as described in the

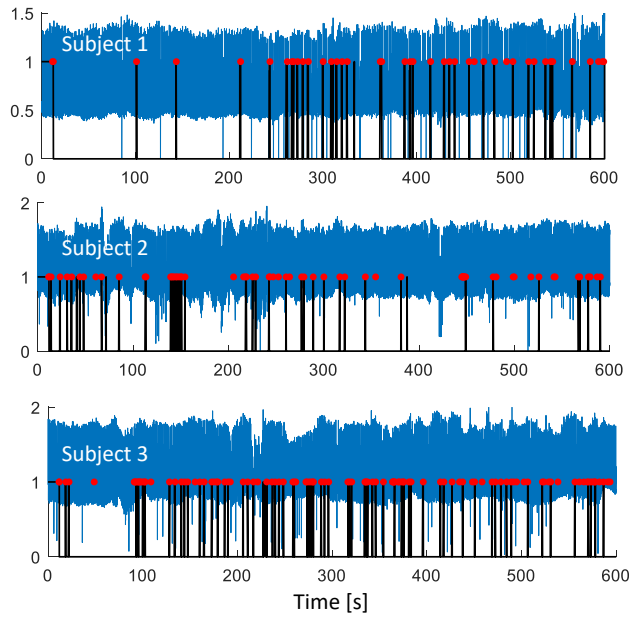

Fig. 11. Sinus arrhythmia detection on ECG data (blue) of three subjects from MIT-BIH database [39-40]. The pulses (black) created by the cardiac processor timestamps the arrhythmia events annotated in the recordings (red dots).

TABLE I
ARRHYTHMIA DETECTION PERFORMANCE

Subject	TP	FN	Se
P1 (Rec 114)	33	0	100%
P2 (Rec 210)	49	3	94.2%
P3 (Rec 214)	87	5	94.5%

TABLE II
FEATURE DETECTION PERFORMANCE

Subject	R-R Error	SBP Error	SpO_2 Error
S1	29.9 ± 57.5 ms	-1.8 ± 2.5 mmHg	5.1 ± 4.8 %
S2	24.8 ± 22.7 ms	1.24 ± 6.1 mmHg	7.3 ± 7.7 %
S3	24.1 ± 46.8 ms	-7.4 ± 6.4 mmHg	5.6 ± 5.3 %

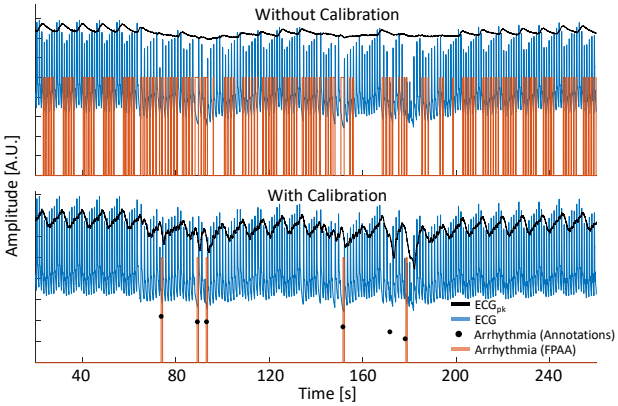

Fig. 12. The calibration of the cardiac processor is achieved through FG programming. In arrhythmia detection, a significant improvement is achieved with the calibration.

Physionet Database. Over the course of ten minutes ECG datasets from three subjects true/false positive values and the positive predictive values for PVC and rhythm changes are summarized in Table I. A normal resting heart rate is 60 to 100 beats per minute (bpm). Arrhythmia events considered occur if HR reduces below 40 bpm or elevates to more than 140 bpm [41]. In these cases, the minimum deviations between two consecutive R-R intervals in an abnormal decrease and increase in HR can be 500 ms (HR: 60 bpm → 40 bpm) and 172 ms (HR: 100 bpm → 140 bpm), respectively. Our processor can detect minimum R-R interval variations greater than 50 ms. For each subject, we achieve detection sensitivity of at least 94.2%. Other low-power arrhythmia detection algorithms demonstrate detection sensitivities comparable to ours [42-43]. It should be noted that, in our processor, a factor affecting the arrhythmia detection is the amplitudes of the R-waves. To illustrate, some of the arrhythmia events missed by our processor are short normal R-waves followed by tall abnormal R-waves. In that case, while the normal short R-wave is missed by the peak detector, the abnormal tall R-wave is tracked, which in some cases results in a normal R-R range. In future implementations, the arrhythmia detection can be made directly on pulses timestamping the detected R-waves, thereby potentially improving the arrhythmia detection sensitivity.

Additionally, SBP values obtained from the FPAA processor and a digital MATLAB algorithm, namely find peaks, finding the local maxima of the ABP waveforms in a given heart beat are compared. Lastly, SpO2 calculations of the FPAA processor and digital calculations implemented on MATLAB are compared. These results are summarized in Table II. Percentage mean R-R errors for the subjects S1, S2, and S3 are 2.95%, 3.75% and 3.55%; respectively. Mean SBP calculation errors are 1.67% (S1), 1.06% (S2), and 6.27% (S3). SpO2 variation over time is inherently prone to high-frequency noise due to the division operation involved. Therefore, the mean percentage SpO_2 errors in the Table II have been found after low-pass filtering both the analog (cardiac processor) and digital (MATLAB) SpO_2 outputs by a 4th order FIR filter (f_{-3dB}= 1 Hz). Despite the good correlation between the SpO_2 calculations of the analog circuitry and the DSP algorithms for the healthy subjects, there is a systematic error created by the dc offset of the V_{mid} in Fig. 8. In future implementations, this offset can be removed by modifying the circuit to perform multiplication/division on current signals with zero offset [44]. Despite the good correlation between the SpO_2 calculations of the analog circuitry and the DSP algorithms for the healthy subjects, there is a systematic error created by the dc offset of the V_{mid} in Fig. 8. In future implementations, this offset can be removed by modifying the circuit to perform multiplication/division on current signals with zero offset [44]; and thus, potentially reduce the SpO_2 errors to comply with the FDA guidance for pulse oximeters [45].

FG offers flexibility in terms of calibrating a mixed-signal system and mitigating the intrinsic mismatch present in a system. From the perspective of a system analyzing physiological and vital signs, this would enable healthcare workers to tailor/tune the system to meet the needs of a patient. Analog algorithm implementation on the FPAA enables controlling several parameters [34, 46]. Calibration is largely

TABLE III
COMPARISON OF FPAA AND FPGA

System Block	FPAA Power Consumption	FPAA Area (Number of CABs)	FPGA Power Consumption	FPGA Area (Number of Logic Elements)
ECG R-R and arrhythmia detect	126 nW	1 CAB (ECG R-R) 3 CABs (Arrhythmia)	10 µW	254 Logic Elements
SBP and DBP measurement circuitry	251 nW	1 CAB	3 µW	48 Logic Elements
SpO_2 monitoring	1.44 µW	5 CABs	50 µW	672 Logic Elements
Cardiac Processor Total	1.82 µW	10 CABs	63 µW	974 Logic Elements

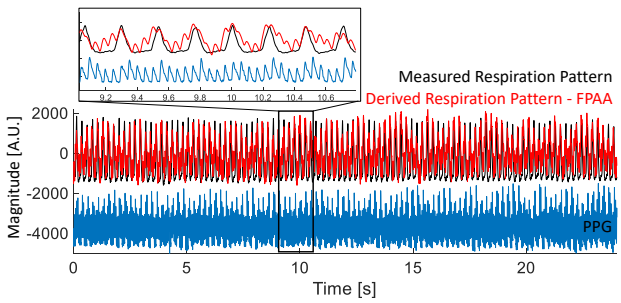

Fig. 13. Low-pass filtered peak detector output from a PPG signal can extract the respiration pattern.

done in two ways. In the first type of calibration [46] the parameters are stored in a LUT format which can be used for subsequent programming of an FPAA. This calibration is for programming different FPAAs with the same high-level infrastructure. Parameters involve the bias voltages of the FG, time for tunneling and electron injection from or on to the floating node. Secondly, in a run time mode a BIST [34] system is used for tuning the circuits to certain specifications. For instance, we tune the offset of the FGOTA comparator, measured during runtime and followed by programming cycles, in Fig. 10 to obtain the results of the Fig. 12. The data recorded from different subjects will vary and hence it would necessitate subject specific calibration, similar to the performed for cochlear implants. Notably, the digital signal conditioning stage limits the signal amplitudes to 1 V_{pp}, and thus enabling subject-specific parameters to be calibrated for different subjects and recordings.

In this study, the focus has been given to three vital signs. However, the circuit architectures presented in this work can be used in monitoring other vital signs or cardiac features. For instance, the R-R monitoring approach can be expanded to monitor other periodic vital signs such as the respiration rate. Changes in intrathoracic pressure during inhalation and exhalation modulates the stroke volume and therefore amplitude of PPG signals, which reflects the changes in blood volume [47]. Therefore, to monitor the respiration rate, the peak value of one of the PPG signals can be LPF by a G_m-C filter with a sub-Hz cutoff frequency to obtain the respiration pattern. The similarity between the extracted respiration pattern following that procedure and measured respiration pattern by a pneumatic respiration transducer are displayed in Fig. 13. For respiration rate calculation, the respiration waveform can be fed to a hysteretic differentiator followed by a comparator for generating pulses at the peaks.

The input dynamic range for the ECG, ABP, and PPG signals is ~1 V_{pp}. For validation of the computation electronics, signal conditioning has been performed in the digital domain. However, as an ultimate localized processor solution, signal conditioning may be achieved in the analog domain on the FPAA chip [48].

Table III shows the power consumption of analog components of the proposed system implemented on a reconfigurable and programmable analog platform. The Table III also shows the dynamic power consumption of the

TABLE IV
PERFORMANCE COMPARISON

	Processing Domain	Type/ Technology	Processing and Features/Accuracy[a]		Power Consumption
			R detect	Arrhythmia detect	
This Work	Analog	FPAA SoC/ 350 nm	Yes/ Se: 94.2% (R) AE=3.4% (R-R)	Yes/ Se: 96.2%	0.126 µW
[49]	Analog (Feature Extraction) Digital (Heartbeat detection)	ASIC/ 180 nm + DSP chip	Yes/ N/A	No	0.8 µW (Feature extraction)
[50]	Digital	ASIC/ 350 nm	Yes/ +P:99.57% (R)	No	0.96 µW
[51]	Digital	ASIC/ 65 nm	Yes N/A	Yes/ PA: 86%	2.78 µW
[52]	Digital	ASIC/ 180 nm	Yes/ +P:100% (R)	No	43 µW
[53]	Digital	ASIC / 180 nm + DSP chip	Yes/ N/A	Yes/ DA: 97.25%	459.967 µW
[54]	Digital	ASIC/ 65 nm	Yes/ +P:99.49% (R)	No	770 mW

[a]Se:Average Sensitivity; AE:Average Error; +P=Positive Predictive Value; PA:Prediction Accuracy; Power consumption in [54] was calculated based on provided energy (0.11 mJ) and frequency (7 kHz) values.

corresponding system implemented on a digital FPGA, fabricated on a 180 nm CMOS process and supplied by 3.3 V. The digital implementation computes with an 8-bit accuracy and clock frequency of 10 kHz. The power consumption is first-order estimate generated using PowerPlay Power Analysis tool provided by Intel for power estimation of Altera FPGAs. Additionally, the Table III shows the area utilization for an FPGA and the FPAA. The area for FPAA is noted in terms of CABs whereas for an FPGA it is noted in terms of logic elements. Logic elements of the FPGA, specifically the one used for comparison, consists of four-input Look-Up-Table (LUT) and a programmable register. It should also be noted that the FPAA consists of 98 CABs and the FPGA used here consists of 1270 logic elements.

To evaluate the performance, a comparison of the cardiac processor with the state-of-the-art real-time cardiac signal processing approaches is presented in Table IV. Cardiac processing in the state-of-the-art approaches are either purely in digital or mixed-signal domains. The processor presented can detect R-peaks with a sensitivity of 94.2% and arrhythmia with a sensitivity of 96.2% from ECG while outperforming the power performance of the most power-efficient digital ASIC alternative [50] by consuming ~87% less power. Two factors contribute to the power efficiency; (i) computing in the physical domain and (ii) facilitating the CMOS subthreshold region. Computing in the physical domain leads to simplicity. For instance, dc blocking, differentiation, and noise-suppression tasks are performed by a single hysteretic differentiator implemented using a FGOTA. To minimize the power consumption, majority of the devices are operated in subthreshold region by biasing via sub-nA currents.

Energy efficiency of the LED drive, sensing, and signal-conditioning electronics has been the focus of the efforts on design of wearable/implantable SpO_2 monitoring electronics. Among these studies, the ones computing perfusion index ratio in real-time commonly use microprocessors with current consumption values comparable to average current consumption of the LEDs, which is the highest power consumption block of a PPG sensing system [55-57]. One study in the literature demonstrates low-power real-time perfusion-index ratio computation [58]. Performing the computations in the analog domain, the signal processing circuitry in [58] consumes ~200 µW, which is more than two orders of magnitude higher than the power consumption of the SpO_2 monitoring electronics of the cardiac processor presented.

Our approach of implementing the biosignal processing algorithms in the analog domain on an FPAA can be expanded to designing a custom analog-processor leveraging FG devices for programmability. Notably, the FG-programming in the FPAA processor is performed once to tune the parameters. Therefore, in a custom FG-based solution, the peripheral blocks needed for FG programming (e.g., ADC, DAC) can be designed to be detachable from the processor during the processing to minimize the footprint.

V. Conclusion

This paper presents design and validation of an analog signal processor for energy-efficient vital sign monitoring at cardiac signal sensor node. The processor extracts important features from ECG, ABP, and PPG signals to detect the vital signs, compresses the cardiac signals in a physiologically-relevant manner, and generates warning signals in the events of sinus arrhythmia and low SpO_2 levels. The processor is implemented on an FPAA hardware embodying a programmable and reconfigurable FPAA chip and an on-chip microprocessor. The system performs the calculations in real-time. In addition, the analog R-R and SpO_2 outputs are logged to PC when an abnormality is detected, thus enabling further analysis offline. For energy efficiency, the circuitry has been designed in CMOS subthreshold region of operation. The system has been demonstrated using datasets from healthy subjects and patients and analog computation results match with offline processing outputs obtained by MATLAB algorithms. We envision the processing approach and circuit details detailed in this study laying the foundation for addressing the needs of the cardiac health sensor nodes of the future body sensor networks.

VI. Acknowledgment

The authors would like to thank Omer Inan and the members of the Inan Research Lab at Georgia Tech for assistance with data collection from healthy subjects and sharing the data.

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